ATCZ175 InterOP

SDR Interference Emulator

Preliminary specification

16.12.2020

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1 Overview

The SDR Interference Emulator (SDR-IE) is a powerful modular Software Defined Radio (SDR) platform that provides wireless communications designers an affordable means for developing communication systems such as interference emulation and measurements, radio frequency testing and many more. The SDR-IE refines user experience making SDR prototyping more accessible by delivering the optimum balance between simplicity and performance. It is ideal for a wide range of application areas and as an alternative for widespread SDR produced by Ettus research and National instruments (NI).

The SDR-IE features high-performance FPGA SoC and supports variety of commercially available RF front ends from NI/Ettus[1] for various frequency bands and applications. Figure 1 displays the SDR interference emulator. The 250 MS/s sampling frequency makes this device suitable for spectrum sensing with >200 MHz frequency bandwidth as well as for cognitive radio applications.

Figure 1: SDR Interference Emulator

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[1] Front end modules supported in the firmware as of 16.12.2020: NI WBX

2 Specification

The SDR Interference Emulator consists of three main parts:

1. **The SDR mother board**: The main board contains all necessary parts to connect all accessories together meaning the daughter board, FPGA module and other 3rd party accessories through the GPIO connector. The board also contains all connectivity interfaces (USB, PCI, Ethernet, GPIO, JTAG, power etc.)

2. **The FPGA and processor module**: To keep maximum modularity of the system the SDR emulator allows to use various Xilinx FPGA modules, depending on the user requirements. All modules in FPGA design are easily and clearly described, the usage of standard Xilinx IP cores, AXI stream and AXI lite buses allows the simplest integration of your own DSP modules. The Direct Memory Access (DMA) between FPGA logic and ZYNQ processor system allows to implement real time application.

3. **The daughter board**: The daughter board is the HW part which is used for signal down-conversion of the Radio-Frequency (RF) analog signal to the Base-Band (BB) analog signal. Also, in point of view of the system modularity as a daughter board can be used commercially available equipment from Ettus (WBX, SBX, CBX see [2]) or specific designed daughter board by user.

Table 1: Key parameters

Interface	**Power supply**	9 – 15 VDC / 35 W Power DIN-4 connector
	PC connectivity	USB 2.0 (serial) Ethernet 1G
	Connectivity	GPIO (Cannon DB-15) RS-232 (Cannon DB-15) SD card slot (on board)
	RF connectors	Ref In (10 MHz) TX1 (Daughterboard) RX1 (Daughterboard)
HW	**ADC**	250 MS/s 14/16 bits[2] SFDR 85 dBc
	DAC	250 MS/s (internal oversampling x2) 16 bits SFDR 85 dBc
	Tuning range	WBX: 50-2200 MHz, SBX: 10-6000 MHz
	Architecture	homodyne[3]
	Frequency synthesis	Coherent full-duplex, or Independent TX/RX frequency
	FPGA	ZYNQ Ultrascale+
	Supported FPGA modules	Trenz Electronic TE0803
	QSPI flash	128 MB
	RAM	2/4 GB DDR4 (64-bit width)[4]
	Slice LUTs free/used	341000
	Slice registers	682000
	BRAM	31.5 MB
	DSP	3528
	Processor	Quad-core ARM® Cortex™-A53 MPCore™ up to 1.5GHz Dual-core ARM Cortex-R5 MPCore™ up to 600MHz
	Frequency accuracy	10 ppm 1 ppm (with TCXO option)
	Operating system	PetaLinux
SW	**Operation**	Standalone or host-controlled
	Host SW programming	GNU OCTAVE / MATLAB C++

The SDR Interference Emulator consists of three main parts:

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[2] assembly options

[3] frontend specific

[4] dependent on the selected FPGA module

Signal streaming is implemented using TCP packets. The throughput is 730 Mbit/s of net data upstream and 730 Mbit/s of net data[5] downstream simultaneously, which corresponds to 22 MSa/s of 2x16-bit complex IQ samples.

Table 2: Mechanical specification

Parameter	Value	Unit
Dimensions (L x W x H)	24 x 17 x 5.8	cm
Weight	1.25	kg

3 Environmental Conditions

Ambient temperature range   23 °C ± 5 °C

Relative humidity range   10% to 90%, noncondensing

4 Acknowledgement

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[5] after removing packets overhead