ATCZ175 INTEROP PROJECT

Pilot Study on Analysis and Modeling of Co-Site Interference onto Future Airborne Communications Systems LDACS

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Contents

List of Figures

List of Acronyms

ADC	Analog-to-digital Converter
ADS-B	Automatic Dependent Surveillance-broadcast
APT	Airport
AWGN	Additive White Gaussian Noise
BER	Bit Error Rate
CNS	Communications, Navigation, and Surveillance
CPLD	Complex Programmable Logic Device
DME	Distance Measuring Equipment
DUT	Device Under Test
EEPROM	Electrically Erasable Programmable Read-only Memory
ENR	En-Route
ETH	Ethernet
FIS-B	Flight Information Service-broadcast
FL	Forward Link
FPGA	Field Programmable Gate Array
GNSS	Global Navigation Satellite System
I^2C	Inter-integrated Circuit
IF	Intermediate Frequency
InterOP	Interoperability of Heterogenous Radio Systems
JTIDS	Joint Tactical Information Distribution System
LDACS	L-band Digital Aeronautical Communication System
LNA	Low Noise Amplifier
LO	Local Oscillator
LOS	Line of Sight
MIDS	Multifunctional Information Distribution System
NATO	North Atlantic Treaty Organization
NB	Narrow-Band
NF	Noise Figure
NLOS	No Line of Sight
OCXO	Oven Controlled Crystal Oscillator
OFDM	Orthogonal Frequency-division Multiplexing
PCB	Printed Circuit Board
PLL	Phase-locked Loop
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase-shift Keying
RF	Radio Frequency
RL	Reverse Link
RX	Receiver
SAW	Surface Acoustic Wave Filter
SESAR	Single European Sky Air Traffic Management Research Program
SF	Super-Frame
SNR	Signal-to-noise Ratio
SSR	Secondary Surveillance Radar

TCAS	Traffic Collision Avoidance System
TIS-B	Traffic Information Service-broadcast
TMA	Terminal Maneuvering Area
UAT	Universal Access Transceiver
VNA	Vector Network Analyzer

Chapter 1

Introduction

This report concerns about the impact of communications, navigation, and surveillance (CNS) systems in the L-band onto the upcoming L-band Digital Aeronautical Communication System (LDACS). The spectral efficiency of the deployed CNS systems is very poor, thus, LDACS is designed as overlay system in the L-band. Due to the legacy systems, LDACS is exposed to high power co-site interference. This report shows the tremendous impact of the interference on the LDACS receiver (RX) prototype. Furthermore, different hardware blanking methods to shorten the blanking duration are tested and compared with each other. The compression behavior of the hardware is simulated with the Interoperability of Heterogenous Radio Systems (InterOP) interference models. Those models are used in the LDACS system simulator to predict the impact of a co-site interference for different flight scenarios.

The report is structured as follows. Section 1.1 gives a brief introduction to the LDACS system design, followed by a discussion of the existing interrogators for LDACS in section 1.2. An overview of the implemented LDACS system simulator is given in section 1.3. Section 1.4 presents the LDACS hardware prototype and its various hardware blanking features. Chapter 2 concerns with the measurement environment, followed by the conducted measurement results for the various hardware blanking schemes. The interference simulations with the embedded InterOP interference model are compared with the conducted measurements in chapter 3.

1.1 LDACS System Design

Eurocontrol predicts that the number of flights will increase by 50% till the year 2040 [1]. This will increase the data exchange for the existing aeronautical communications systems significantly. Those communication systems are the bottle-neck for the future airtraffic, since they are not capable to handle the amount of data. Additionally it is planed to adjust flight plans in real-time e.g., by changing weather conditions, the clearance of a normally restricted flight zone, or any other unexpected reasons, which in fact increases the data exchange tremendously. The procedure is termed 4-D trajectory operation [2] within the Single European Sky Air Traffic Management Research Program (SESAR). The fourth dimension represents the dimension time and refers to the time scheduling in real-time for each flight phase of an aircraft. To fulfill 4-D operation, the interconnection of several different systems is necessary and LDACS represents one of these systems to successfully provide this feature.

LDACS is a terrestrial cellular based communication system, with purpose to exchange data between a ground station and an aircraft. The system will be deployed in the aeronautic L-band ranging from $960\,\mathrm{MHz}$ to $1215\,\mathrm{MHz}$. The transmission scheme is orthogonal frequency-division multiplexing (OFDM) based, with an effective channel bandwidth of $\approx 500\,\mathrm{kHz}$ and a channel spacing of $500\,\mathrm{kHz}$ [3]. A ground station sends data and control information via the so-called forward link (FL) to the aircraft. All ground stations are synchronized with each other and build the common time reference for the communication system. The link from the aircraft to the ground station is termed reverse link (RL) and carriers data from each registered aircraft. Both links a synchronized with each other and have the Super-Frame (SF) depicted in Fig. 1.1 as the smallest common frame type. As mentioned in the introduction chapter 1, LDACS will be deployed as overlay system between existing CNS systems. The utmost goal is not to disturb the existing legacy systems. On the contrary the same is not true for LDACS, which will be exposed to high power interference scenarios discussed in section 1.2. Table 1.1 gives an overview of the most important LDACS parameters.

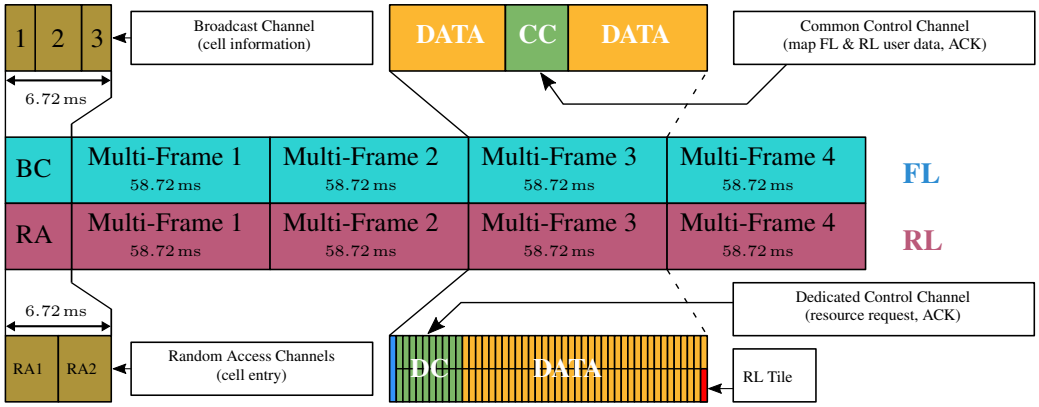


Figure 1.1: LDACS Super-Frame structure

Table 1.1: LDACS system parameters

Parameters	**Values**
Type	OFDM
Modulations Schemes	QPSK, 16QAM, 64QAM
max. Data Rate FL	$\approx$1.42 Mbit/s
max. Data Rate RL	$\approx$1.1 Mbit/s
Total Channel Bandwidth	625 kHz
Effective Channel Bandwidth	$\approx$500 kHz
Subcarriers	64 (50 used) $\Delta F = 9.765\,625$ kHz
Useful Symbol Duration T_U	102.4 µs
Cyclic Prefix Duration T_{CP}	17.6 µs
OFDM Symbol Duration T_S	120 µs
SF periodicity	240 ms
FL Frequency Band	1110 MHz – 1156 MHz
RL Frequency Band	964 MHz – 1010 MHz
LDACS Channel Spacing	500 kHz
max. Cell Size	200 NM

1.2 L-band Legacy Systems and LDACS Interrogator

This section presents the existing interferer for LDACS, with a focus on the worst case interference scenario. Fig. 1.2 depicts the currently usage of the CNS systmes in the aeronautical L-band and the planed deployment of LDACS colored in green. The L-band adjoins at lower frequencies to the mobile telephone communication standards, on the upper edge its limited by the Global Navigation Satellite System (GNSS), which operate with low power and thus, it is sensitive to interference. The universal access transceiver (UAT) is a data link, which is designed for flight information service-broadcast (FIS-B), traffic information service-broadcast (TIS-B) and also automatic dependent surveillance-broadcast (ADS-B), to provide e.g., weather graphics, real-time positions of nearby aircraft, potential proximate intruder, any many other information. A recommendation for the use of UAT is given in the distance measuring equipment (DME) standard [4]. The secondary surveillance radar (SSR) is an active radar for aircraft identification like ADS-B or traffic collision avoidance system (TCAS). Since, these systems are essential for a safe air traffic no other systems are allowed for the specified frequencies. Furthermore, the DME standard reserves explicitly the frequency range for SSR [4]. Joint Tactical Information Distribution System (JTIDS) and multifunctional information distribution system (MIDS) are digital military data links used by the North Atlantic Treaty Organization (NATO), they are also known as Link 16. These links use a frequency hopping scheme within in the L-band with a 3 MHz channel separation [5]. Link 16 has a „guest“ state within the L-band, since the purpose of the aeronautical L-band is civil aviation [6]. Thus, JTIDS and MIDS are no immediate interferer to the LDACS system.

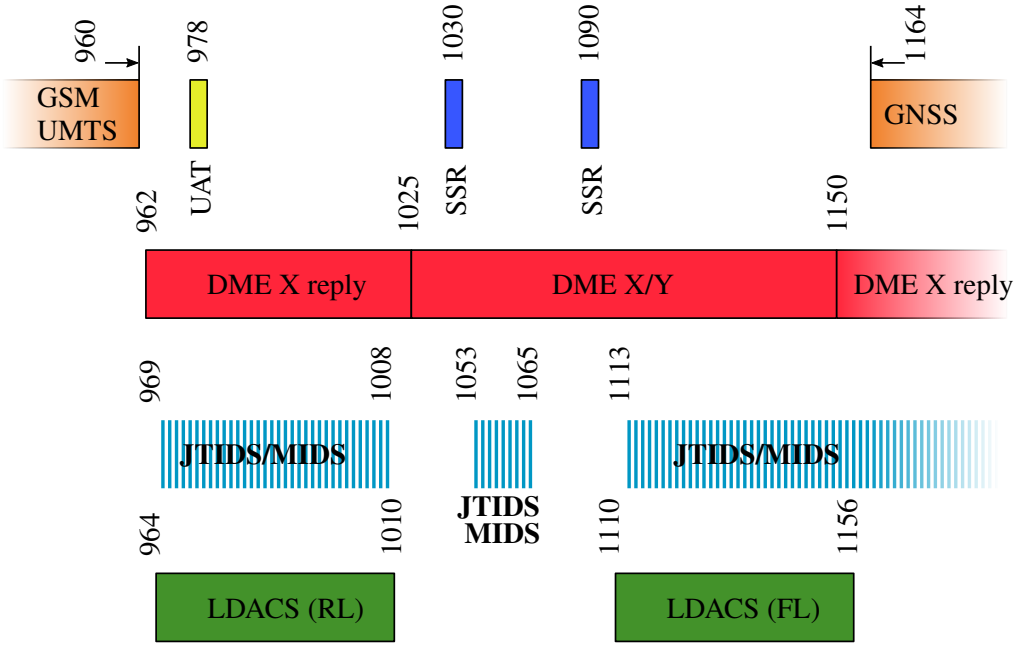


Figure 1.2: L-band usage and LDACS deployment

The worst case interferer for LDACS is the DME. As depicted in Fig. 1.2, the DME occupies the complete aeronautical L-band, with the mentioned exception above. Some frequency slots are currently not used but for future use reserved. DME is used to measure the aircraft distance to a ground station beacon. For this purpose the aircraft DME transmitter sends a Gaussian shaped pulse-pair towards an DME ground station. The beacon repeats the double pulse after a fixed time delay. The reply frequency is $\pm 63\,\mathrm{MHz}$ in respect to the aircraft transmit frequency depending on the transmission mode. By statistically evaluation of the ground station replies, an aircraft DME receiver is able to distinguish between its replies and those of other aircraft. In search mode an aircraft transmits up to $150\,\mathrm{ppps}$, when it found its reply answer it goes over into tracking mode with a maximum repetition rate of up to $30\,\mathrm{ppps}$. The DME system is divided in $1\,\mathrm{MHz}$ slots with a channel bandwidth of $\approx 1\,\mathrm{MHz}$. One problem with the DME standard is that the requirements to generate a pulse-pair is very loose e.g., the pulse width, rise and fall time. These parameters have severe impact on the spectral efficiency. The spectral shape of the pulses is Gaussian. LDACS will be deployed between the DME channels, where the side lobes already decayed in comparison to the main lobe. The problem with this approach is that the transmit power of a civil DME transmitter can be as high as $1\,\mathrm{kW}$ and for military versions up to $10\,\mathrm{kW}$, which will result in a strong interference scenario

for the LDACS system.

1.3 LDACS System Simulator

The implemented system simulator is based on the actual LDACS standard [3] and is entirely programmed in *Matlab*. The simulator comprises the complete physical layer of the LDACS standard, higher level functions e.g., handover scenarios and dynamic aircraft allocation, are not implemented. The simulator can be split into three independent parts, as depicted in Fig. 1.3.

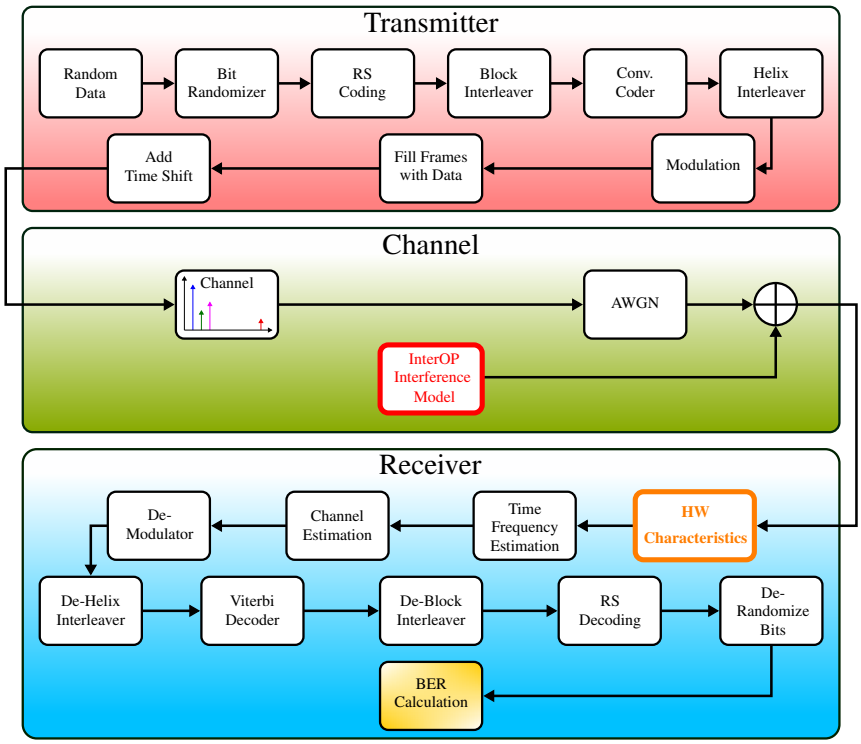


Figure 1.3: Block Diagram of LDACS System Simulator

The transmitter part, generates random data, which is encoded accordingly to the link and frame type (see Fig. 1.1). The smallest simulation frame type for FL and RL is one SF. Within the SF all link dependent frame types with different coding schemes are included. The simulation results in chapter 3 the focus is only on the Data payload. Furthermore, the simulator includes all defined modulation and all possible coding schemes [3].
The second part are the channel models, which can be applied to the signal. The LDACS standard defines three different channel models. Those models cover the following flight scenarios for an aircraft:

1. Airport (APT) channel → defined for taxiing and parking at the airport, with no line of sight (NLOS) component, because of shadowing, due to ground infrastructure or trees.

2. Terminal Maneuvering Area (TMA) channel → designed for landing and approach scenarios, with a line of sight (LOS) component and many scatterer, because of the low flight level of an aircraft.

3. En-Route (ENR) channel → represents an aircraft at its cruising altitude and speed, with a strong LOS component and only a few scatterer.

After the channel is applied to the signal, additive white Gaussian noise (AWGN) according to the defined signal-to-noise ratio (SNR) is added. At this stage the interference from the InterOP model are randomly added to the signal.
The third part is the receiver. It contains the hardware characteristics of the LDACS prototype, like the compression behavior of the RX front-end over input power levels and the radio frequency (RF) to intermediate frequency (IF) frequency response. Compression behavior is modeled as look-up function for magnitude and phase with respect

to the input power. The characteristics are applied onto the input signal. Afterwards, time and frequency offset is estimated, via the synchronization symbols and the frequency response is equalized in this stage. Furthermore, the SNR is estimated, which has an impact for the soft-decision Viterbi decoder. Subsequently, channel estimation is done by an inverse weighting method over the time/frequency grid of consecutive OFDM symbols. The used method is the so-called Shepard's method [7]. The interpolation grid in time and frequency direction is selectable, which has an impact on the computational complexity. Afterwards follows demodulation, de-interleaving and decoding of the received signal. The received data is compared with the sent one to determine the bit error rate (BER).
An important component of the receiver part is the reliable DME impact detection. Although the DME pulses are short compared to the length of an OFDM symbol, the consequence of an undetected DME pulse is rather fatal. The reason therefore is manifold. First of all the demodulated signal is corrupted and is somewhere randomly in the I/Q plane, thus, the decoded OFDM symbol is for sure wrong. The interference has also an enormous impact on the channel estimation, because the estimation will fail if pilots symbols are destroyed. Unfortunately, this affects several following symbols, depending on the interpolation grid. Furthermore, the Viterbi algorithm will tend to a wrong decoding sequence, if the soft-decision symbol is declared as most likely, because the SNR is wrongly predicted as too high.

1.4 LDACS Receiver Front-end Hardware

This chapter gives a brief introduction of the developed LDACS receiver prototype. For a better explanation of the RX unit, a block diagram is depicted in Fig. 1.4. The prototype is designed for airborne as well as ground station operations. It consists of a baseboard indicated in green, which splits the input signal into two RF paths to enable the possibility to equip two RX modules. This feature is required for the airborne RX. One RX module is locked and registered to the ground station in the current located cell, while the other one scans for adjacent ground station cells. This gives the opportunity to switch quite fast between two cells for a hand-over procedure and additionally enables the possibility for ranging. Since LDACS is designed as an overlay system in an already used frequency band (see Sect. 1.2), it is mandatory for the RX unit to withstand high input power, due to co-site interference. At the start of the development phase the mandatory maximum tolerable input power at the RX input port was defined with $25\,\mathrm{dBm}$. The subsequent low noise amplifier (LNA) can withstand powers up to $27\,\mathrm{dBm}$, which would make additional input protection obsolete. At the end of the development phase the specification for the maximum input power has been changed to $30\,\mathrm{dBm}$, thus, an additional input protection of the RX front-end is necessary to prevent damage of the subsequent components. For input power monitoring a power detector with a high-impedance tap is placed at the RX input. If the input signal exceeds a predefined threshold, the subsequent RF switch can be toggled to 50Ω to protect the circuitry and furthermore, to reduce the saturation time of the components. The blanking signal for the RF switch is also used as information for the Viterbi decoder, to mark the "damaged" OFDM symbols with erasures, to distinguish if the trellis paths are trustworthy for each decoding step.

Additionally an oven controlled crystal oscillator (OCXO) with $40\,\mathrm{MHz}$ clock rate is placed on the baseboard to provide a stable reference for the RX phase-locked loops (PLLs). The clock reference is distributed for up to five external devices e.g., measurement equipment.

Fig. 1.5 shows the developed LDACS RX hardware prototype. In comparison with Fig. 1.4, it consists of a baseboard module indicated in green and two RX modules indicated in red. This prototype concept gives the opportunity to select and evaluate different RX modules. For evaluation a narrow-band and a broad-band concept was elaborated. The narrow-band RX is split into two separate module, depending on what link type (FL or RL) is selected. The reason therefore is that the narrow-band RX uses the same PLL for both link and operates, either with a low-side local oscillator (LO) for the RL or with a high-side LO for the FL. The separation in two individual modules is necessary, because depending on the link type high-side or low-side noise is down converted to the IF, what would tremendously increase the RX noise figure (NF). To circumvent this effect filtering before the conversion stage is necessary.
An additional concept is to use a broadband RX module, which has the advantage to receive multiple LDACS ground stations at the same time. This gives the opportunity for a fast hand-over and the triangulation of the actual position of the aircraft via all received ground stations. Furthermore, the concept with aircraft to aircraft communication could be reconsidered, which was part of the initial LDACS standard draft. One drawback of the broadband RX is the higher vulnerability to interrogator compared to the narrow-band RX version. This

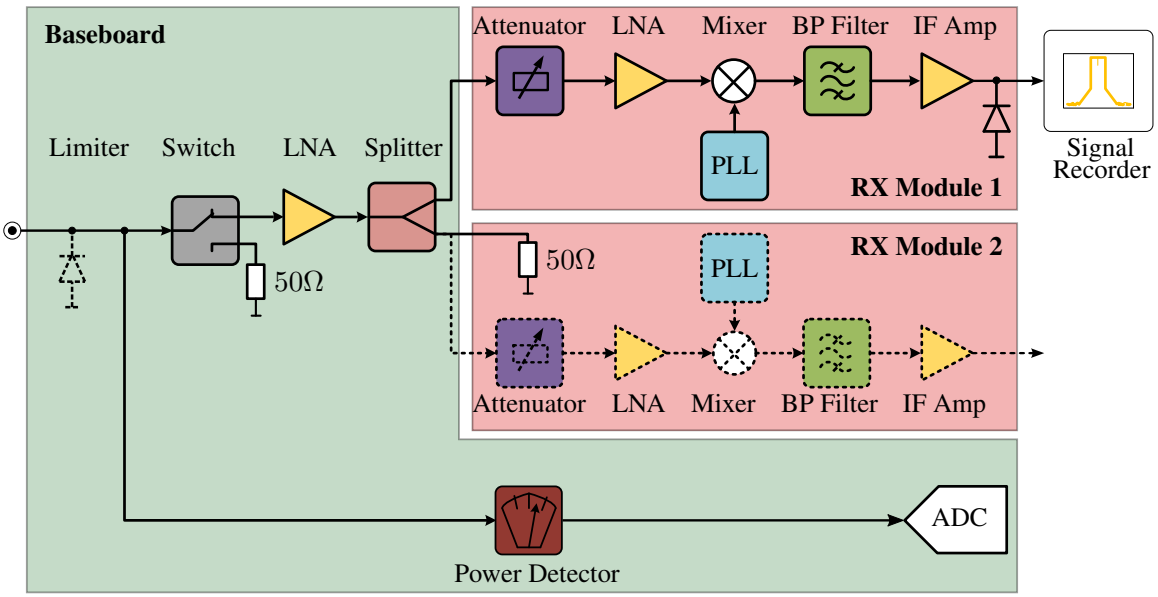


Figure 1.4: Block Diagram of LDACS receiver Prototype

investigation and comparison is not part of this report.

The attenuator onboard the RX modules are controlled via a parallel interface, which has the advantage to change the attenuation within $\approx 60\,\mathrm{ns}$. This gives the additional opportunity to protect the subsequent hardware and prevent it from long term compression.

Figure 1.5: LDACS Receiver Hardware

Each board is equipped with an inter-integrated circuit (I^2C) electrically erasable programmable read-only memory (EEPROM) to store gain over frequency and the RF to IF response of each RX module. This is necessary, since the ripple of IF filter, especially of the narrow-band modules can not be neglected and has to be compensated. The EEPROM also contains the deviation of the digital attenuator. Via the attenuator setting and its deviation, the total gain from RF to IF is known and it is possible to calculate the received signal power.

Chapter 2

Interference Measurements Setup and Results

This chapter starts with the introduction of the measurement setup for the interference measurements. The subsequent sections present the conducted measurement for different hardware options and hardware blanking methods. The measurements build the basis for simulations with the used InterOP interference model. The worst case interrogator for LDACS is the DME (see Sect. 1.2), which is used as interference signal. The test conditions for hardware and simulation (see Chapt. 3) are listed in Table 2.1. For the conducted measurements, only one RX module is equipped on the baseboard. The second RF path is terminated with $50\,\Omega$, which is indicated with the dashed lines for the RX module in Fig. 1.4.

Table 2.1: Measurement and Simulation Settings for FL

Parameters	**Settings**
Link Type	FL
Modulations	QPSK
Convolutional Coding	1/2
Channel Type	AWGN
LDACS frequency	$1110.0\,\mathrm{MHz}$
Used RX module type	Narrow-band
Interrogator Type	DME
DME frequency	$1110.5\,\mathrm{MHz}$
DME pulse repetition	$150\,\mathrm{ppps}$
DME pulse width	$3.5\,\mu\mathrm{s}$
DME pulse separation	$12\,\mu\mathrm{s}$

2.1 Interrogator Measurement Setup

Fig. 2.1 depicts a block diagram of the measurement setup for interrogator measurements. The whole measurement setup is controlled via *Matlab*. As LDACS signal source a SMBV100A signal generator from Rohde&Schwarz is used. The prepared FL signal is fully compliant to the LDACS standard [3], according to Table 2.1 settings. Playback and recording is started from the *Matlab* session and triggered via the field programmable gate array (FPGA). The combination of analog-to-digital converter (ADC) and FPGA is fully implemented to down-convert the IF signal from the RX to baseband. The combination is used as signal recorder. The initial step for each measurement is to determine the trigger delay between signal source and signal recorder, which is necessary for a synchronized measurement. The combination of AMIQ and SMIQ from Rohde&Schwarz build the interrogator source for the LDACS RX. The interrogator is triggered randomly by a microcontroller with a duty cycle of $150\,\mathrm{ppps}$. The output pulses have to be amplified by an external amplifier to obtain the required peak pulse power of $30\,\mathrm{dBm}$. One drawback of this measurement is that the noise floor changes with the required peak power of the pulses. Thus, the comparison between simulation and measurement get rather tedious. Furthermore, this scenario would be quite unusual, because that would result in a permanently enhanced noise floor when using an DME

transmitter. As a consequence the DME transmitter is turned off when nothing is transmitted. For this purpose a RF switch is placed after the DME amplifier to turn the output off when no interrogator is triggered. The output power of the DME transmitter is adjusted with a step attenuator. The LDACS signal and the interrogator are combined via a splitter and connected to the RX input. The logic analyzer records the detected interrogators from the device under test (DUT). This information is used for erasure decoding in a further step. The microcontroller has the additional task to configure the DUT for the different hardware blanking modes.

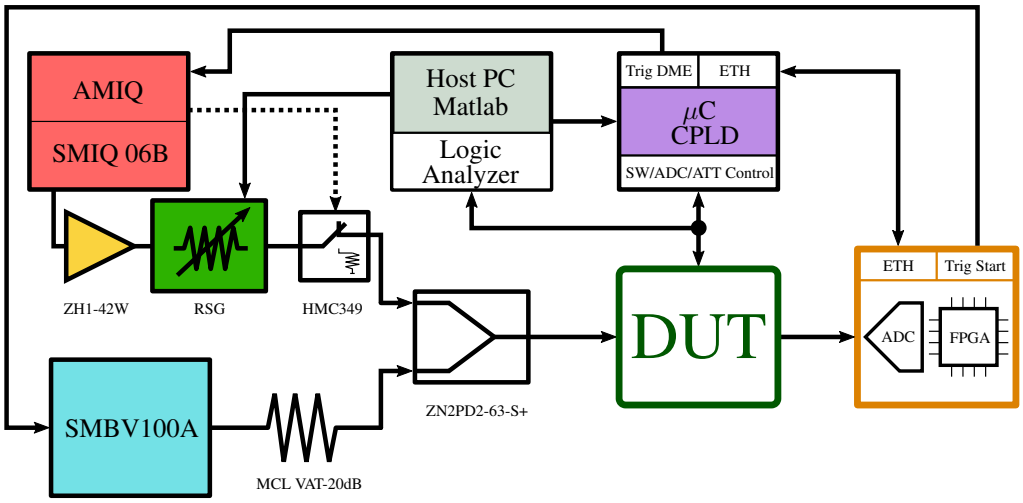


Figure 2.1: Measurement Setup for Interrogator Influence on BER

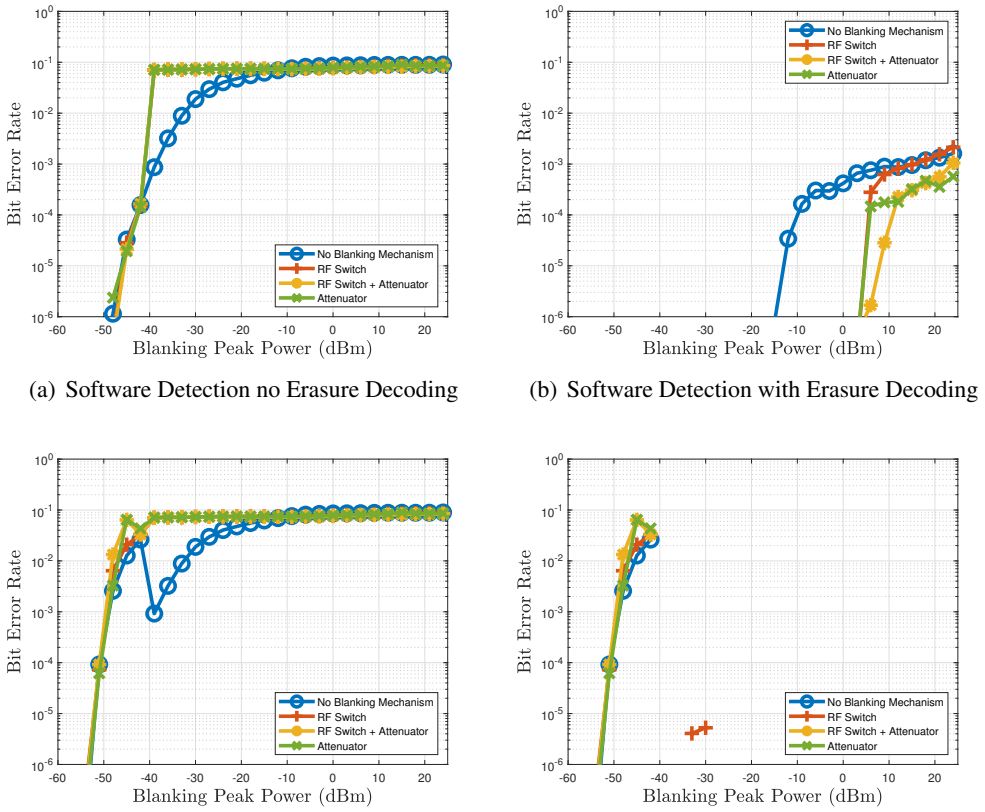
Different blank methods are supported by the hardware when an interference is detected by the front-end power detector. The blanking methods are listed below with reference to the block diagram Fig. 1.4:

1. no hardware blanking; switch always set to RF through; attenuator setting unchanged
2. switch opens, when interrogator exceeds blanking threshold; attenuator setting unchanged
3. switch opens, when interrogator exceeds blanking threshold; attenuator is set to maximum
4. switch always set to RF through; attenuator is set to maximum

2.2 Measurement Results

The measurements are conducted for the highest receiver sensitivity for an LDACS signal of $-104\,\mathrm{dBm}$ [3]. The interrogator is placed with an offset of $500\,\mathrm{kHz}$ next to the wanted signal. This corresponds to the worst case blanking scenario for the LDACS receiver, since the Gaussian shape of DME pulse does not decay that fast. Furthermore, it is assumed that the aircraft is in search mode for an DME beacon, which corresponds to a pulse repetition rate of up to $150\,\mathrm{ppps}$. For this measurement the peak blanking power is varied from $24\,\mathrm{dBm}$ down to $-80\,\mathrm{dBm}$.

The evaluation of the received signal consists of four different decoding/estimation schemes. One scheme tries to detect DME impacts via an increased in-band power level compared to the average power level of the received OFDM signal. If the power level exceeds a certain threshold a DME impact within the OFDM symbol is very likely. This scheme is termed “software detection” in this report. The detection information is used in two ways. On the one hand pilot carriers within an OFDM symbol are marked and excluded for channel estimation (see Sect. 1.4), on the other hand also the data carriers are marked as erasures for the decoder, to prevent a wrong decoding path. The second scheme uses the blanking information from the front-end power detector to identify the distorted OFDM symbols. This scheme is termed “hardware detection” in this report.



(a) Software Detection no Erasure Decoding

(b) Software Detection with Erasure Decoding

(c) Hardware Detection no Erasure Decoding

(d) Hardware Detection with Erasure Decoding

Figure 2.2: NB-RX with Output Limiter for DME Interrogator

2.2.1 Blanking Measurement Narrow-Band RX

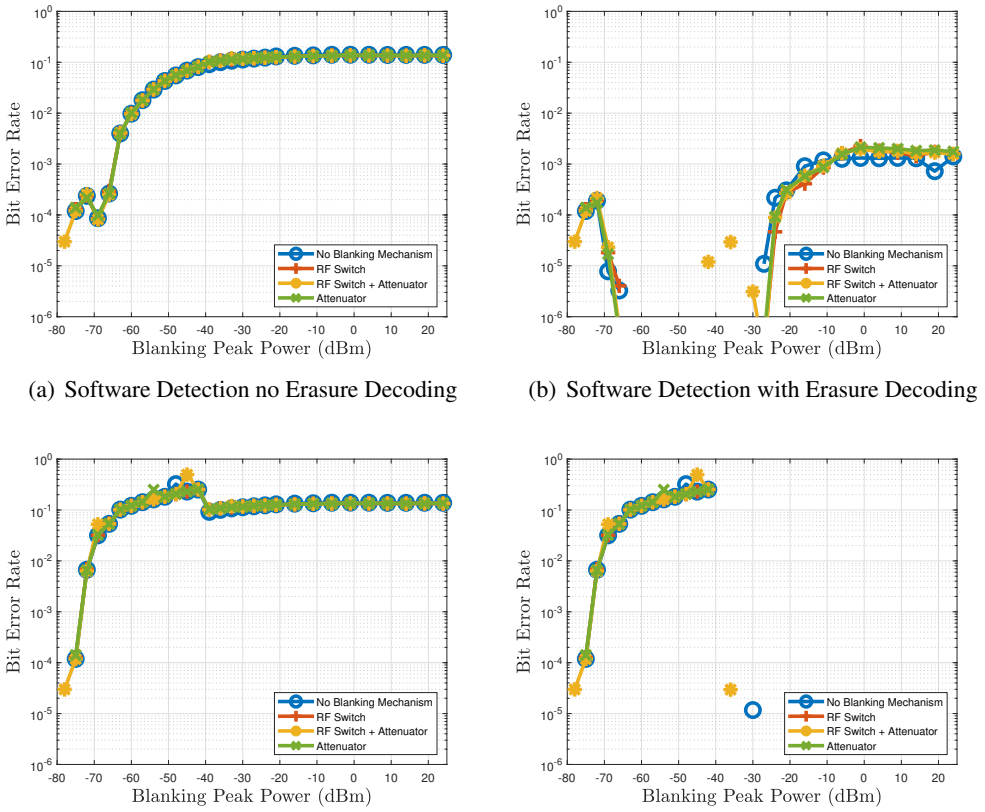
This subsection shows the impact of an DME and a pulsed interrogator onto the Narrow-Band (NB) RX hardware with different hardware blanking methods. Two different assemblies of the hardware are examined. One with a limiter at the output of the NB module (see Sect. 2.2.1.1). The output limiter is necessary that the subsequent ADC module is not damaged. The second assembly has an additional limiter at the RX input (see Sect. 2.2.1.2). The output limiter is still necessary, because the RX has enough gain to amplify the limited input signal over the maximum input ratings of the ADC.

2.2.1.1 Output Limiter Diode

For this measurement a limiter diode is mounted at the output of the RX to examine the effect of the interrogator on the RX chain. Fig. 2.2 depicts the four different detection and decoding schemes, in regard of the different hardware blanking types.

Fig. 2.2(a) shows the decoding result for detecting the interference by software. The distorted pilot symbols are marked for channel estimation, but the knowledge of the distortion is not used for erasure decoding. The figure shows that for the “No Blanking Mechanism” the lower the peak power of the interrogator gets, the better becomes the BER. This figure also reveals the ratio between the necessary average LDACS power and the peak power of an interrogator to achieve a certain BER, when software blanking detection is used. The discontinuity to the other modes is due to the blanking threshold of the front-end ADC. One can see that the impact of the hardware blanking has a tremendous impact on the decoding. It is obvious that for this decoding scheme, without the use of erasures, the signal is even more distorted by the hardware protection than it would be by the interrogator.

Fig. 2.2(b) depicts the BER for the case that the DME distortion is detected by software and the information is also used for erasure decoding. The evaluation shows that the impact of the interrogator is much less to the RX, than it is without the erasure decoding. Furthermore, the different blanking modes show an improvement of the BER of almost 20 dB, compared to “No Blanking Mechanism”. Thus, it can be concluded that the hardware blanking methods relax the blanking duration of the RX chain. This decoding scheme also shows that there is



(a) Software Detection no Erasure Decoding

(b) Software Detection with Erasure Decoding

(c) Hardware Detection no Erasure Decoding

(d) Hardware Detection with Erasure Decoding

Figure 2.3: NB-RX with Output Limiter for Pulsed Interrogator

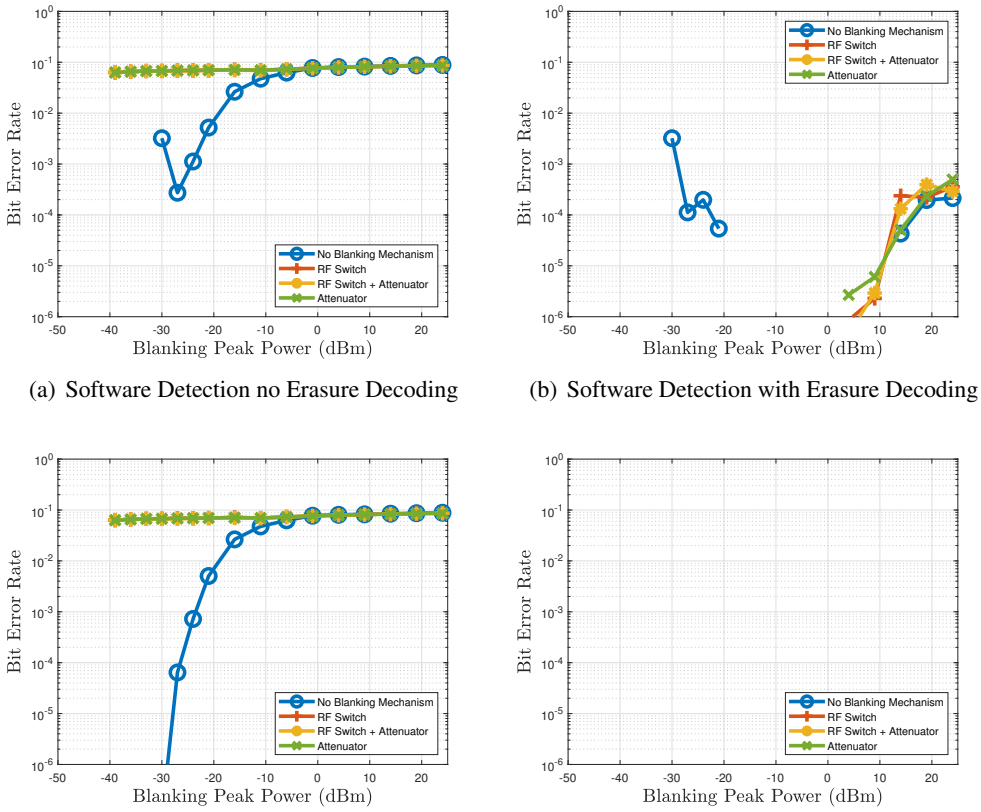
no big difference between setting the RX attenuation to maximum or by switching the input signal to $50\,\Omega$, if a distortion is detected. A minor improvement occurs when both concepts are combined.

Fig. 2.2(c) shows the BER results with hardware blanking detection. For this scheme the information is only used to mark pilots for channel estimation, it is not used for erasure decoding. The scheme shows bad decoding results, especially when the front-end ADC is not able to detect the interrogators the BER gets even worse. Fig. 2.2(c) gives an additional important result. It shows the necessary relative power ratio between the average power of the LDACS signal and the peak power of the DME pulse to achieve a certain BER, without knowledge when the interference occurs.

Fig. 2.2(d) presents the BER results with hardware blanking detection combined with erasure decoding. The results are remarkable good. Regardless what blanking mode is used, no bit error occurs in the detection range of the front-end ADC. Even when no blanking mechanism is used, the indication of the distorted OFDM symbols is enough for the Viterbi decoder to prevent bit errors. One minor drawback is that the detection range is about $15\,\mathrm{dB}$ too less, that the interference has no impact on the BER for the highest sensitivity level of the LDACS receiver.

The requirement that co-site interrogator will have no influence on the BER is the combination of blanking detection in software as well as in hardware. This can be concluded in regard of Fig. 2.2(b) and Fig. 2.2(d). The combination of both methods gives an error free reception. The error free overlap of both methods is quite large and spans over more than $20\,\mathrm{dB}$. This is gives the opportunity to define a relaxed threshold, at which point either of the methods is in charge to mark erasures. It is also possible to combine both information with each other to ensure a correct interference detection.

Now the question arises when to select either the “software” or the “hardware” detection method? Fortunately, there are two ways to detect the threshold to switch form one scheme to the other. Since the software solution compares the average in-band LDACS power with the power for each OFDM symbol, it is possible to derive an estimate of the blanking power. The in-band blanking power will vary dependent on the peak power of the interrogator. The hardware solution gives the same information, but in a different way. Dependent on the peak power of the interference the hardware indicates a blanking signal as long as the threshold is exceeded. The blanking duration indirectly implies the peak power of the DME pulse. The peak power detection for both methods



(a) Software Detection no Erasure Decoding

(b) Software Detection with Erasure Decoding

(c) Hardware Detection no Erasure Decoding

(d) Hardware Detection with Erasure Decoding

Figure 2.4: NB-RX with Output Limiter for DME Interrogator 1 MHz

can be used at which threshold the receiver should either select the “software” or the “hardware” detection.

The measurements in Fig. 2.2 have shown the impact of an DME pulse-pair on the RX with a rise time of about 2.5 µs for various hardware blanking methods. Fig. 2.3 depicts the impact of a step function with a rise time of less than 300 ns on the RX hardware. As the figure shows, the impact of the step function has a tremendous influence on the BER.

The ratio between LDACS average power and the maximum interrogator power for software detection method without erasure decoding is about 25 dB worse (see Fig. 2.3(a)) compared to the DME interferer (see Fig. 2.2(a)).

Fig. 2.3(b) shows the BER with erasure decoding for the software option. The necessary ratio between wanted and unwanted signal also reduces about 15 dB. The bad BER result for low interrogator powers can be ignored, because the measurement setup had a problem for several minutes of recording.

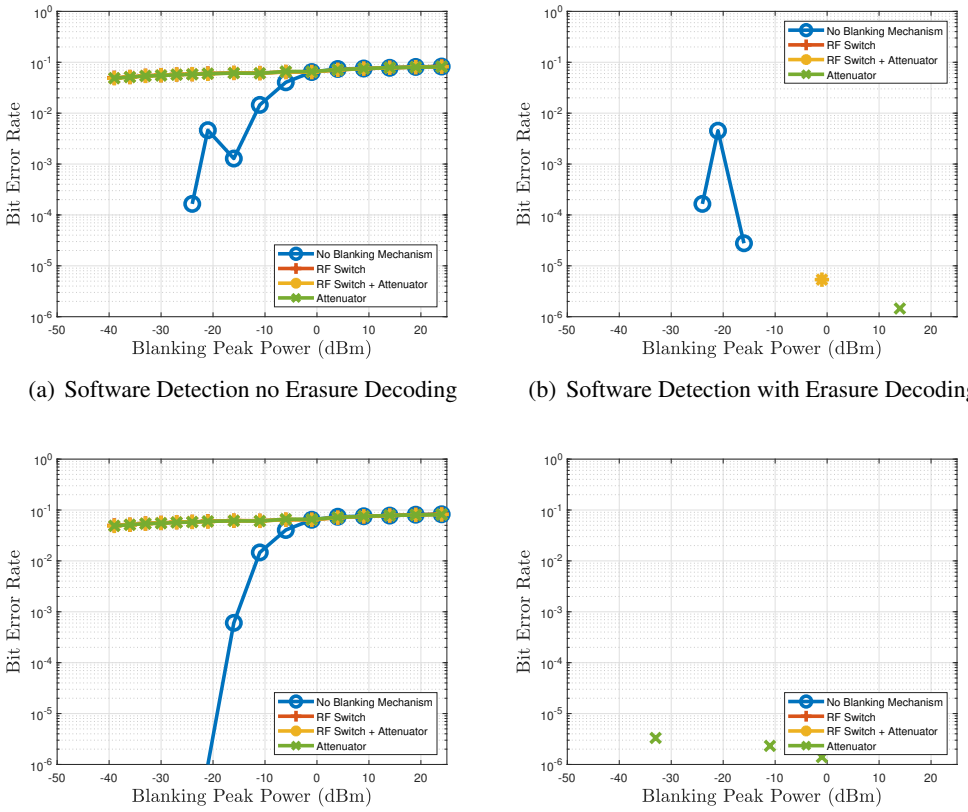
The hardware detection method without erasure decoding depicted in Fig. 2.3(c) shows that the pulsed interference has a strong impact on the BER.

The hardware detection with erasure decoding shows very good performance in regard of a pulsed interrogator (see Fig. 2.3(d)). As long as the front-end ADC is able to detect the interrogator, all blanking methods operate quite good. Below the detection threshold the BER is extremely high. The combination of software and hardware method is again the preferred option. Although the gap for error free reception between both options is reduced, it is still a headroom of 10 dB available.

For the sake of completeness the impact of an DME interrogator was test for a frequency offset of 1 MHz and 2 MHz relative to the LDACS signal.

Fig. 2.4 shows that the influence of the interference is reduced. The ratio between the interference peak power to the LDACS mean power increases about 20 dB. This results in an error free detection for the hardware detection with erasure decoding (see Fig. 2.4(d)).

With a separation of 2 MHz the interference to LDACS power ratio increases by an additional 10 dB (see Fig. 2.5(d)).



(a) Software Detection no Erasure Decoding

(b) Software Detection with Erasure Decoding

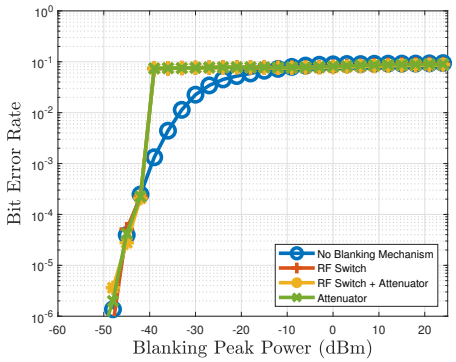
(c) Hardware Detection no Erasure Decoding

(d) Hardware Detection with Erasure Decoding

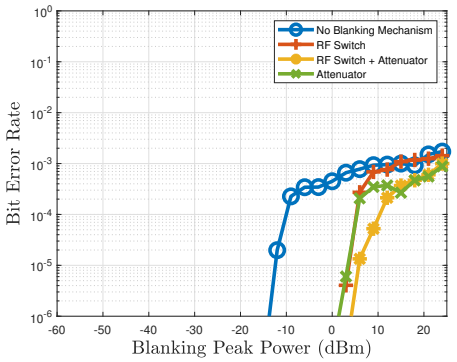
Figure 2.5: NB-RX with Output Limiter for DME Interrogator 2 MHz

2.2.1.2 In/Output Limiter Diode

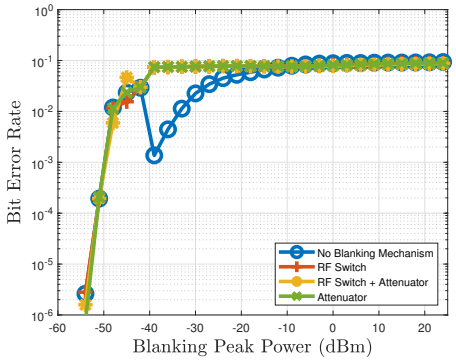
In this subsection an additional limiter diode was placed at the input of the receiver. The idea is to reduce the compression duration of the first LNA, due to DME interference. Fig. 2.6 depicts the measurement results for all presented blanking methods. Unfortunately, the figures show no further improvements for a DME interrogator with a limiter diode at the input of the RX module. The same is true for a pulsed interrogator, depicted in Fig. 2.7.



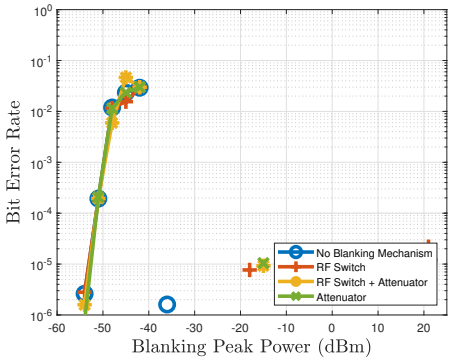
(a) Software Detection no Erasure Decoding



(b) Software Detection with Erasure Decoding

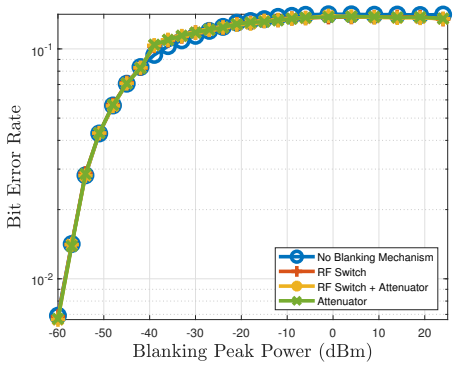


(c) Hardware Detection no Erasure Decoding

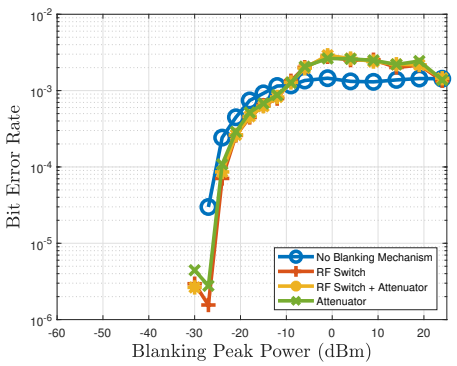


(d) Hardware Detection with Erasure Decoding

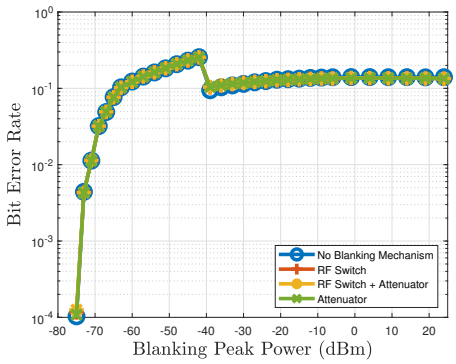
Figure 2.6: NB-RX with In-/Output Limiter for DME Interrogator



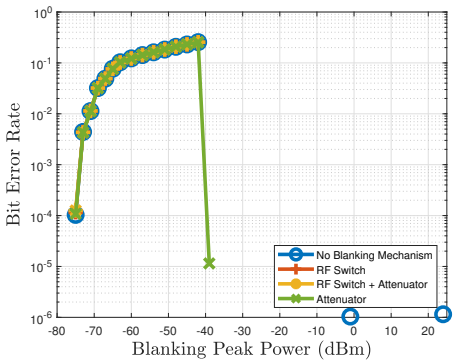
(a) Software Detection no Erasure Decoding



(b) Software Detection with Erasure Decoding



(c) Hardware Detection no Erasure Decoding



(d) Hardware Detection with Erasure Decoding

Figure 2.7: NB-RX with In-/Output Limiter for Pulsed Interrogator

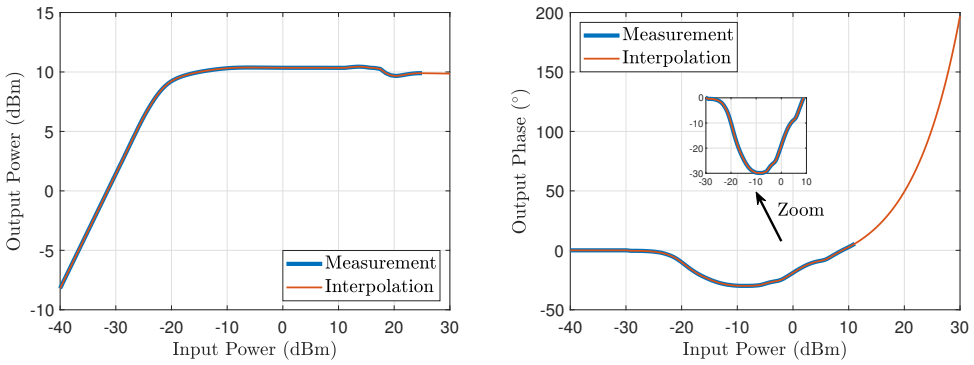
Chapter 3

Interference Simulation Results

To simulate the impact of a DME interrogator onto the LDACS RX front-end, the well defined InterOP interference models have been used within the LDACS system simulator. One important point is the modeling of the compression behavior of the RX front-end hardware, with the goal to keep the model as simple as possible. The modeling of the saturation is rather tedious, since the front-end is driven into strong compression. The different stages of the RX will saturate at different input powers, which is a dynamic process and represents an unpredictable behavior. In the first section of this chapter the modeling of the compression behavior based on measurements is given (see Sect. 3.1). The subsequent sections show the simulation of the BER with the InterOP interference framework, compared to the conducted measurements. Starting with the compression behavior of a single limiter diode, followed by the examination from the RF input to the splitter output of the LDACS RX (see Fig. 1.4), concluding with the complete RX front-end from RF input to IF output.

3.1 RX Compression Measurement and Modeling

The input/output response of the RX front-end for the LDACS system simulator is modeled by a look-up table. In a first attempt the compression of the RX was measured with a power meter by varying the input power. This gives the static compression behavior of the output in respect to the input power. The phase component was assumed to be unchanged. Simulation results have shown that the measurement and the simulation do not fit. Especially around the point where the saturation commences, a big mismatch occurred. Therefor it was necessary to extend the look-up table by a input power dependent phase term. The phase deviation of the RX chain was measured with the vector network analyzer (VNA) N5247A from *Keysight*, which has the measurement option for AM/AM and AM/PM measurements. The output power of the VNA is limited to the maximum of $14\,\mathrm{dBm}$. To extend the measurement range for magnitude interpolation the measurement results from the VNA and the power meter have been combined. The phase component is extrapolated for higher input powers. This is valid, since the RX front-end is already highly non-linear and the carriers of the corrupted OFDM symbols are completely distorted



(a) Magnitude (b) Phase

Figure 3.1: Measurement and Look-up Model of RX compression behavior

in magnitude and phase. Figure 3.1 shows the AM/AM and AM/PM measurement of the RX from RF input to IF output. The compression of the magnitude is depicted in Fig. 3.1(a), it clearly shows that the output power is clamped to 10 dBm, due to the limiter diode at the IF output. The phase deviation is shown in Fig. 3.1(b). It depicts that the phase is starting to deviate before the magnitudes 1 dB compression point is reached.

The compression behavior for section 3.1.2 and 3.1.3 was measured individually with same the measurement setup as explained above, the results are not depicted in the report.

3.1.1 Memory Effect of the Limiter Diode

As preparation for the simulations in section 3.1.2 and 3.1.3, the memory effect of a limiter diode was tested. This is necessary, since the modeling with a look-up table is only valid, if the limiter shows no or only a minor memory effect. For this purpose the effect of a step response was tested onto the limiter diode.

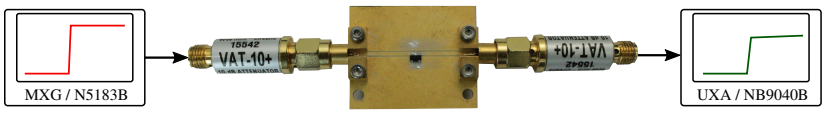
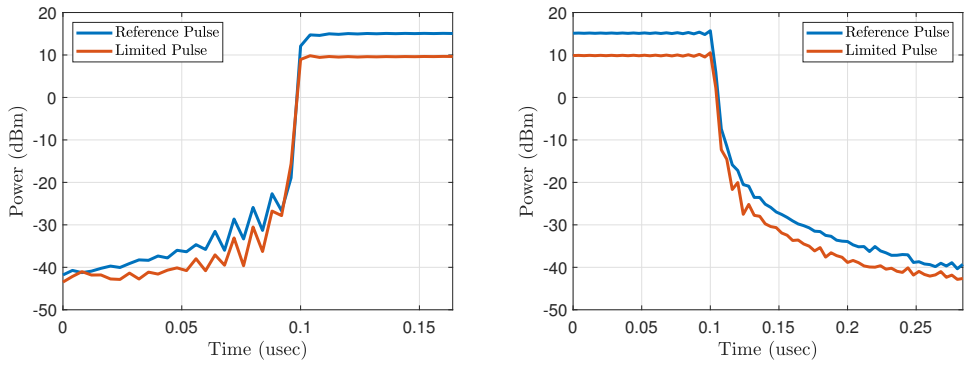


Figure 3.2: Measurement Setup for Memory Effect Test

The test setup to measure the memory effect of the limiter diode is depicted in Fig. 3.2. The printed circuit board (PCB) consists of a 50 Ω line, terminated with a 10 dB attenuator on each side to prevent reflection of the test pulse when the diode starts to conduct and provokes a mismatch for the pulse source and the signal recorder.

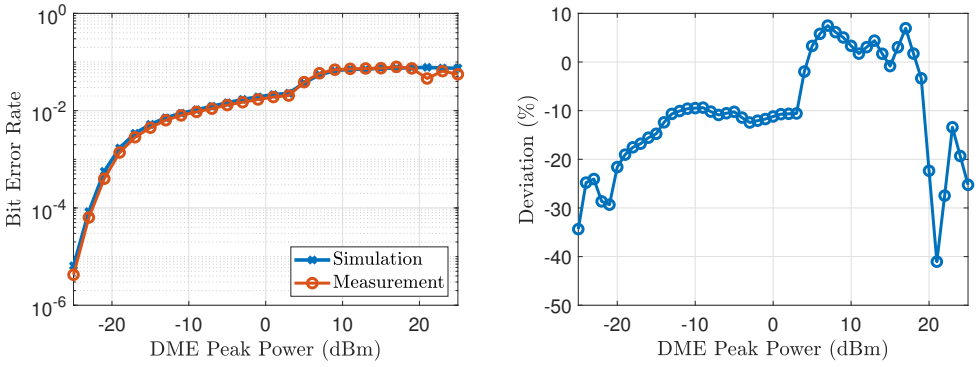
Subsequently, the test procedure is explained in detail: At the beginning, the input pulse is measured with a signal recorder without the clamping diode. This first measurement is used as reference to compare the measurement with the mounted clamping diode. The rise/fall time of the signal generator is typically 7 ns with a >80 dB On/Off ratio. The used signal recorder has a sampling rate of 250 MHz, that results in temporal resolution of 4 ns, which is high enough to sample rising and falling edge of the input pulse. The second measurement is conducted with the limiter diode on the same board. For this purpose the diode is clamped onto the test board. This prevents any change of the measurement setup e.g., by replacing the test board and the effect of unscrewing the test PCB. This results in a maximum deviation of one sampling point, due to the trigger delay between the signal generator and the signal recorder. In Fig. 3.3 the measurement results for the rising and falling edge of the pulse are presented. The pulse is limited to 15 dBm, since the maximum leveled output power of the signal source is 26 dBm. Together with the cable losses and the necessary matching attenuator the input peak power is limited to 15 dBm. An additional amplifier in front of the DUT would alter the measurement results, since the amplifier itself has a memory effect. As depicted in Fig. 3.3, the limiter diode has no identifiable memory effect. There is no recognizable extended decay of the envelope within the 4 ns resolution, neither for the rising edge (see Fig. 3.3(a)) nor for the falling edge (see Fig. 3.3(b)) of the pulse. The measurement results agree with the carrier life time of 4 ns in the data sheet. It can be concluded that the limiter diode itself has no long term impact on the received OFDM symbol.



(a) Rising Pulse Edge

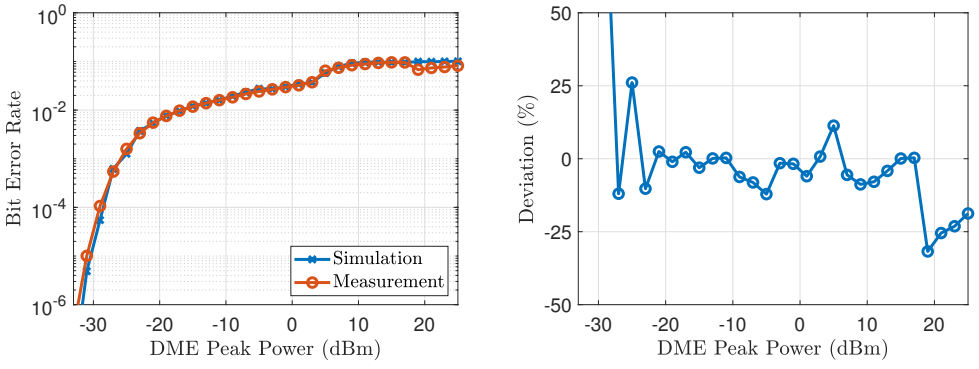
(b) Falling Pulse Edge

Figure 3.3: Measurement of Limiter Memory Effect



(a) BER (b) BER Deviation

Figure 3.4: Limiter Compression, Simulation vs. Measurement



(a) BER (b) BER Deviation

Figure 3.5: Limiter+LNA+Splitter Compression, Simulation vs. Measurement

3.1.2 Blanking Measurement Limiter Diode

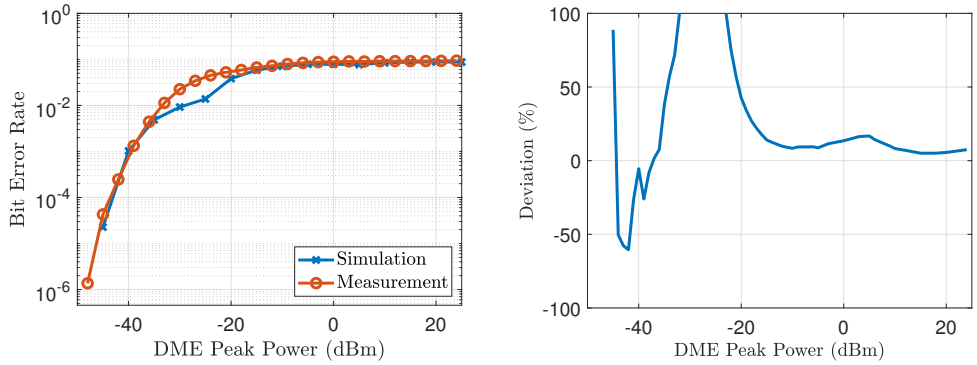
To keep the comparison between the measurement and the simulation simple in a first step, only the compression behavior of a limiter diode was tested. Figure 3.4(a) shows the measurement result for the "software detection" case of the DME interrogator. Only the none erasure decoding scheme is presented. The erasure decoding scheme shows minor errors for the upper power levels, which seems to be a measurement error, because the results show strong fluctuation in the BER. The measurement is depicted in red and the simulation result depicted in blue. Both curves match quite good with each other. The mapping from input to output via the look-up table in the simulator works fine.

3.1.3 Blanking Measurement Splitter Output

This section shows the compression behavior from the RF input to the splitter output. For this measurement the limiter diode at the input was assembled and the second output of the splitter was terminated with $50\,\Omega$. As Figure 3.4 shows the simulation and measurement fit together. Although a LNA is within receiving path, no significant memory effect can be seen. The measurement and the simulation result fit very well.

3.1.4 Blanking Measurement RX Front-end

The verification of the complete RX front-end shows a lager deviation between simulation and measurement compared to section 3.1.2 and 3.1.3. Figure 3.6 depicts the BER simulation and the deviation between simulation and measurement. Especially around the compression point the simulation tends to be better than the measurement. Although the deviation is at a point where the BER is extremely high, it shows that a simple look-up table model does not represent the real behavior of the RX front-end. This leads to the assumption that some components



(a) BER

(b) BER Deviation

Figure 3.6: RX Front-end Compression, Simulation vs. Measurement

after the splitter cause a memory effect of the RX module. Further investigations have shown that the used band-pass filter after the mixer stage, which is a surface acoustic wave filter (SAW), shows strong distortion when an interference occurs. Due to the impulse response of the SAW, the duration of the interference is lengthened, which has a severe impact onto the wanted signal. This explains the measurement effect, why toggling the RF switch and setting the attenuator to its highest attenuation has the same result. Because it has primarily an effect on the blanking behavior of the SAW filter. The modeling of this effect is tedious and a suitable model has not been found yet.

Chapter 4

Conclusion

The report has shown that an error free signal reception for an overlay system is challenging and needs a lot of effort, when operating at the highest RX sensitivity.

As presented in chapter 3 the used InterOP interference models, embedded into the LDACS system simulator are able to reflect the behavior of the RX front-end, when exposed to high power DME interrogators. Only minor deviations between the simulation and the measurements occurred.

It has been shown that the pulse shape has an impact on the compression behavior of the RX front-end. Which leads to the conclusion that the RX from RF input to IF output has a memory behavior.

Furthermore, the importance of a reliable interference detection for the subsequent erasure decoding has been shown. For this purpose two different detection schemes have been presented. The “hardware” detection scheme shows very good BER performance as long as the interference is within the detection range of the front-end ADC. A further extension of the detection range will not be possible, because it would be necessary to decouple more signal power at the RF input, which would increase the NF, resulting in a poor RX sensitivity. The “software” detection scheme works well, but indicates longer blanking duration for higher interrogator powers, which results in a higher BER. Further investigation for an optimal threshold for the “software” variant is necessary. This could be e.g., a varying threshold depending on the LDACS receive power. The combination of both concepts shows the best result for error free reception. Moreover, combining the blanking information of both schemes gives a more reliable and trustworthy interference detection.

The different hardware blanking methods provide an improvement only for the “software” detection scheme in comparison with no hardware blanking. The “hardware” method shows no improvement, since the correct information of an DME impact is enough to ensure an error free BER. Furthermore, the measurement results have shown that the effect of setting the attenuator to its highest attenuation and toggling the RF switch gives the same result. This lead to the conclusion that the down-conversion stage suffers most from the interference. The RF switch can be removed at the input, to improve the overall NF of the RX, since it shows no better performance compared to changing the attenuator settings.

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