FIR filter benchmark

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Goal: Determine maximum clock frequency for Low Pass filter generated by Xilinx FIR compiler.

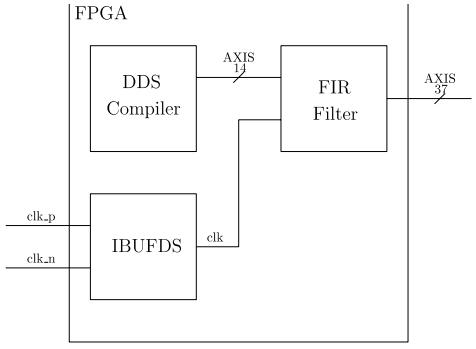
Platform: Zynq UltraScale+ xczu3eg-sfvc784-1-e

Filter order: 166

Introduction:

The SDR under development using two channel 250MSps 14bit ADS42LB49 analog digital converter working with 500MHz clock. The data processing at the FPGA can work on lower clock frequency. The lower digital signal processing frequency resulting into higher resource demands. On the other side maximum frequency is limited by timing of the implemented design. The FIR filter can be one of the timing limiting component. Especially higher order filters can be limiting for whole system. The goal is to determine maximum clock frequency of the FIR filter in our case low pass filter with 166 coefficients and chose DSP clock frequency to fulfill the resource and timing demands with sufficient margin.

Architecture:

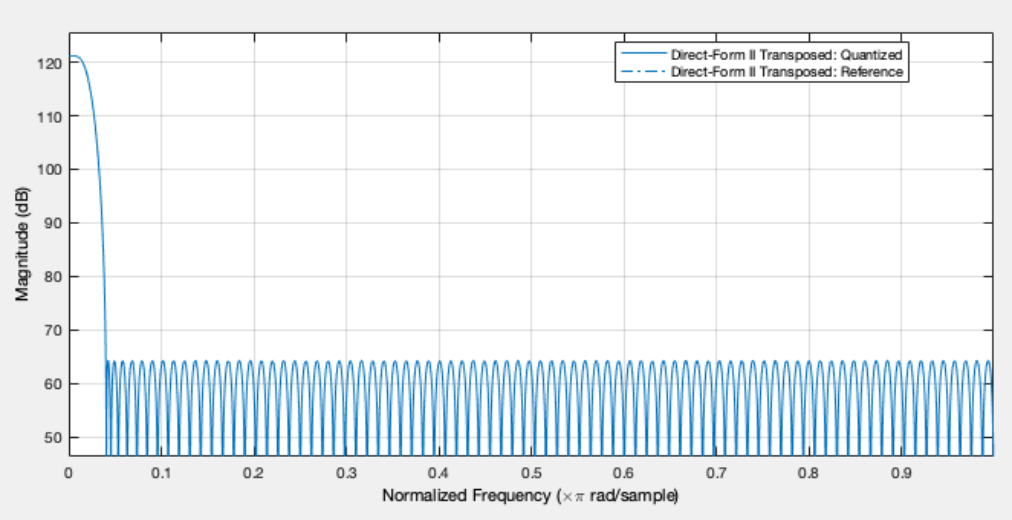


DDC compiler parameters:

System clock (MHz)	500
Number of channels	1
Spurious free dynamic range (dB)	80
Frequency resolution (Hz)	0.4
Phase increment	fixed
Phase offset	none
Amplitude Mode	full range
Output form	twos complement
Output frequency (MHz)	8
Output width	14
Latency	10

DSP48 slice	0
BRAM	1

FIR filter definition:



Desired narrow band LP filter with 166 coefficients

FIR compiler parameters:

Filter type	single rate
Number of interleaved channels	1
Number of parallel channels	1
Clock frequency (MHz)	500
Input sampling frequency (MHz)	500
Coefficients type	signed
Coefficients width	16
Coefficient structure	inferred
Input data type	signed
Input data fractional bits	0
Output rounding mode	full precision
Output width	37
Input FIFO	yes

IO parameters:
Clock input: LVDS
FIR output: LVCMOS18

Conclusion:

To obtain design with maximum clock frequency it is needed to decreasing clock period in several iterations and repeat whole process to generate binary file. The last clock period with proper timing was 1.55ns which is

equal to 645MHz input clock. This result leads to use 250MHz DSP clock to obtain sufficient resources-timing implementation with sufficient margin.